LISTING OF THE CLAIMS

This listing of claims replaces all prior claim listings and versions in the application:

1. (Currently Amended) A portable data storage device operable to write data with reference to a memory address mapping table configured to associate logical address regions with physical address regions, the portable data storage device including:

(i) a data interface for transferring data packets into and out of the portable data storage device[[,]];

(ii) an interface controller[[,]];

(iii) a master control unit[[,]]; and

(iv) ~~at least one~~ a NAND flash memory unit configured to incorporate the physical address regions[[,]];

the interface controller being ~~arranged~~ operable to send data received through the data interface to the master control unit[[,]]; and

the master control unit being ~~arranged~~ operable:

to ~~recognise certain~~ recognize a data ~~packets~~ packet received by the data interface as encoding one of a READ ~~instructions~~ instruction indicating a logical address and ~~other data packets as encoding~~ a WRITE ~~instructions~~ instruction[[:]] indicating the logical address and data to be written;

~~(a)~~ upon receiving [[a]] the READ instruction ~~indicating a logical address~~, to access [[a]] the memory address mapping table ~~which associates logical address regions within a logical memory space with respective first physical address regions within the memory unit~~, to read data from a first physical address in the NAND flash memory unit corresponding, according to the memory address mapping table, to the logical address ~~according to the address mapping table~~, and to transmit to the data interface one or more data packets including the data ~~which was~~ read[[,]]; and

~~(b)~~ upon receiving [[a]] the WRITE instruction ~~indicating a logical address and data to be written to that logical address~~, to determine, as a first determination, [[if]] whether the first physical address ~~corresponding to the logical address according to the memory address mapping table~~ is in ~~the~~ an erased state, and[[:]]

~~if so~~ when a result of the first determination is affirmative, to write the data to be written to ~~that~~ the first physical address, [[or]] and

~~if not~~ when the result of the first determination is negative:[[,]]

(a) to modify the memory address mapping table in accordance with a block queue listing one or more queuing physical address regions to thereby associate a second physical address ~~region~~ with ~~the logical address region containing~~ the logical address, the second physical address belonging to a queuing physical address region at a head of the block queue,

(b) to write the data to be written to [[a]] the second physical address ~~corresponding to the logical address according to the modified memory address mapping table~~, and

(c) to copy any data stored in other ~~potions~~ portions of a first physical address region designated by the first physical address ~~region~~ to corresponding locations of a second physical address region designated by the second physical address ~~region~~.

2. (Currently Amended) [[A]] The device according to claim 1, ~~in which data defining~~ wherein the memory address mapping table is stored as mapping data in the NAND flash memory unit, the ~~memory~~ master control ~~device~~ unit being ~~arranged~~ operable to modify the mapping data upon modifying the memory address mapping table.

3. (Currently Amended) [[A]] The device according to claim 2, ~~in which the~~ further comprising a memory control address unit ~~is arranged~~ operable, upon being initiated, to extract the mapping data from the NAND flash memory unit and to generate the memory address mapping table within RAM memory.

4. (Currently Amended) [[A]] The device according to claim 2, wherein a ~~in which the~~ portion of the mapping data defining ~~the~~ mapping between ~~each~~ a respective physical address region and a logical address region is stored within ~~that~~ the respective physical address region.

5. (Currently Amended) [[A]] The device according to claim 4, wherein ~~in which~~ the mapping data relating to ~~a given~~ the respective physical address region is stored in ~~the~~ a control data storage sector of one or more pages of the respective physical address region.

6. (Currently Amended) [[A]] The device according to claim 1, wherein ~~in which the physical memory space includes:~~

~~(i) physical memory regions associated with logical address regions by the memory address mapping table, and~~

~~(ii) queuing physical memory regions which can become associated with the logical addresses under the operation of the master control unit which modifies the memory address mapping table~~ following said modification of the memory address mapping table, the block queue is modified to place the first physical address at the rear of the block queue.

7. (Currently Amended) [[A]] The device according to claim [[6]] 1, wherein ~~in which~~ the ~~queuing~~ physical ~~memory~~ address regions listed on the block queue are in the erased state.

8. (Currently Amended) [[A]] The device according to claim 6, wherein ~~in which~~ the ~~physical memory space~~ device further includes reserved physical ~~memory~~ address regions which cannot become associated with the logical ~~addresses~~ address under ~~the~~ an operation of the master control unit ~~which modifies~~ when modifying the memory address mapping table.

9. (Currently Amended) [[A]] The device according to claim 1, wherein each ~~in which the~~ physical address ~~regions are~~ region is a respective ~~blocks~~ block of the NAND flash memory unit.

10. (Currently Amended) [[A]] The device according to claim 1, wherein ~~in which~~ the physical address regions ~~are~~ comprise groups of blocks in the NAND flash memory unit, the groups being defined according to a grouping table.

11. (Currently Amended) [[A]] The device according to claim 10, wherein a ~~in which the~~ majority of the groups of blocks ~~are~~ is defined in the NAND flash memory unit according to a rule, and the grouping table defines groups ~~which are~~ positioned in the NAND flash memory unit according to exceptions to the rule.

12. (Currently Amended) [[A]] The device according to claim 11, wherein ~~in which~~ the memory address mapping table contains a flag ~~in respect of~~ for any logical address ~~region which is~~ associated with one of the groups ~~which are~~ of blocks positioned according to the exceptions to the rule.

13. (Currently Amended) [[A]] The device according to claim 10, wherein ~~in which~~ the master control unit associates consecutively following logical addresses within a logical address region with respective pages in different ones of the blocks.

14. (Currently Amended) [[A]] The device according to claim 13, wherein ~~in which~~ the master control unit associates consecutive logical addresses into sets, each of the sets ~~of logical addresses~~ having a number of members equal to the number of blocks in each group, and for each given set the master control unit associates the logical addresses of ~~that~~ the set with corresponding pages of the respective blocks.

15. (Currently Amended) [[A]] The device according to claim 1, wherein ~~in which~~ the master control unit is ~~arranged~~ operable, in response to receiving a first WRITE instruction, to implement the ~~write~~ first WRITE instruction only upon determining that, within a predefined period, a second WRITE instruction ~~is not received~~ obeying a predefined similarity criterion is not received.

16. (Currently Amended) [[A]] The device according to claim 15, wherein ~~in which~~[[,]] following a modification of the memory address ~~modification~~ mapping table in relation to a ~~given~~ first logical address ~~region~~, and prior to said copying of the data from the first physical address ~~region~~ to the ~~new~~ second physical address ~~region~~, said similarity criterion is whether the

second WRITE instruction relates to a logical address corresponding to ~~the~~ a location ~~within~~ designated by the ~~given~~ first logical address ~~region~~ of the data to be copied, and ~~in the case that such a WRITE instruction is received~~ when the similarity criterion is satisfied, aborting said copying operation and instead writing data specified by the second WRITE instruction to ~~the location of~~ the second physical address ~~region~~.

17. (Currently Amended) [[A]] The device according to claim 15, wherein ~~in which~~ the master control unit ~~has~~ is further operable to access [[to]] a data cache and in response to the first WRITE instruction, and to write ~~writes~~ the data to the data cache, said similarity criterion being that the second WRITE instruction relates to the same logical address as the first WRITE instruction, ~~in the case that the determination is positive~~ and when the similarity criterion is satisfied, to write the data specified in the second WRITE instruction ~~being written~~ to the data cache.

18. (Currently Amended) [[A]] The device according to claim 15, wherein ~~in which~~ the master control unit ~~has~~ is further operable to access [[to]] a data cache and in response to the first WRITE instruction writes the data to the data cache ~~provided that~~ when the first WRITE instruction relates to one or more selected logical addresses, said similarity criterion being that the second WRITE instruction relates to the same logical address as the first WRITE instruction, ~~in the case that the determination is positive~~ and when the similarity criterion is satisfied, to write the data specified in the second WRITE instruction ~~being written~~ to the data cache.

19. (Currently Amended) [[A]] The device according to claim 18, wherein ~~in which there are~~ the WRITE instruction relates to a plurality of said selected logical addresses.

20. (Currently Amended) [[A]] The device according to claim 18, further including a pattern recognition unit ~~for recognising~~ operable to recognize as a high frequency logical address a logical ~~addresses~~ address encoded in ~~the~~ WRITE instructions ~~which arise~~ that is received with ~~relatively~~ high frequency, and ~~for setting~~ to set said ~~recognised~~ high frequency logical ~~addresses~~ address as said selected logical ~~addresses~~ address.